

CyberWorkBench®

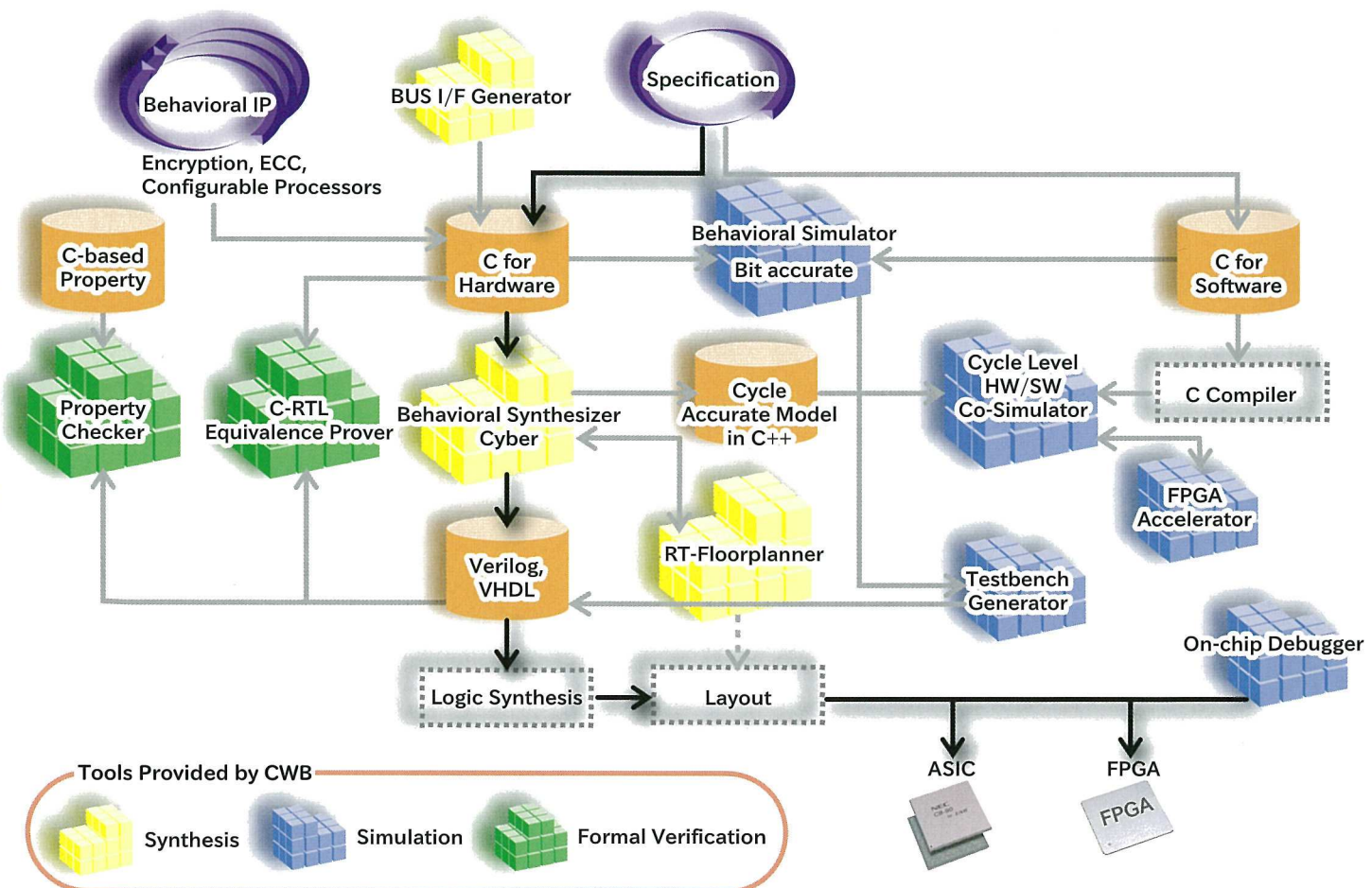
Pioneering C-based LSI Design

CyberWorkBench is the "All in C" synthesis and verification environment for system LSI

□ CyberWorkBench Tool Suites

- Behavioral Synthesizer
Best-in-class synthesis from behavior level description to RTL
- Bus I/F Generator
Automatic generation of AMBA-AHB/AXI/ memory interface
- Cycle Level HW-SW Co-Simulator
Cycle-accurate model generator
Source-level debugger
FPGA accelerator
- C-RTL Equivalence Prover
Guarantees equivalence between behavior level descriptions and synthesized RTL
- Property Checker
Automatic verification of behavior level descriptions
- RT-Floorplanner
feeds back physical information to behavioral synthesis
- Testbench Generator
Automatic testbench generation for cycle-accurate and RTL simulation
- Integrated GUI for Synthesis, Analysis and Verification

All tools are integrated in CyberWorkBench. It allows designers to design and verify their chips all in C-language, without RTL debugging. CyberWorkBench significantly reduces the design cycle, enables embedded SW verification prior to chip fabrication, and delivers extremely reliable design of SoC with high quality results (high performance, small die size and low power).



This is a mature technology proven by shipment of several hundred million dollar SoC per year.

□ Our Advanced Technologies

Behavioral Synthesizer

- Rich experiences of applying to wide variety of real chip designs (cellular phone, digital TV, STB, HDD recorder,...)
*CyberWorkBench is used every day in NEC for developing commercial SoCs making hundreds of million dollar revenue per year.
- Efficient synthesis and high quality of results
- Precise estimation and analysis of QoR
- Easy architecture exploration (various area/performance trade-off)
- Various tuning knobs for SoC design (multiple clocks, sync/async reset, various types of memories, gated clocks,...)
- ANSI-C(enhanced syntax)/SystemC support for design entry (multi-dimensional array, structure, pointer, function, goto, loop,...)

Integrated Tool Set for C-based Design

CyberWorkBench is an IDE, not just a synthesizer...

- Bus I/F generator automatically connects your IP with standard bus (AMBA AHB, AXI, etc...)
- High-speed (10-100x faster than RTL sim.) cycle-accurate HW-SW Co-Simulator and FPGA accelerator, equipped with source-level debugger for HW/embedded SW on ISS
- Simulation model generator for RTL Verilog/VHDL imports legacy IPs into cycle-accurate simulation model (C++/SystemC/SpecC).
- C-RTL formal equivalence prover guarantees the equivalence between C and RTL
- Formal property checker automatically verifies C-based properties
- RT-Floorplanner enables early silicon prototyping to check frequency, routability and power

□ CyberWorkBench's unique features

Specification Language

- ANSI-C (timed/untimed), SystemC, SpecC
- RTL Verilog/VHDL

Outputs

- RTL Verilog/VHDL (synthesizable)
- C++, SystemC, SpecC (fast sim. model)

Target Devices

- ASIC, FPGA

Behavioral Synthesizer

- Efficient synthesis and High QoR
- Precise estimation of area/delay
- Rich analysis capability for synthesis result

System-level Design Tools

- Bus I/F generator
- HW-SW Co-simulator
- RTL power estimator
- RT-Floorplanner

Debug and Verification Tools

- Source code debugger
- C-RTL formal equivalence prover
- Formal property checker

For further information, please contact: info@cad.jp.nec.com

URL: <http://www.cyberworkbench.com/>